(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **11191298 A**
(43) Date of publication of application: **13.07.1999**

(51) Int. Cl **G11C 16/04**
G11C 16/06, H01L 27/115, H01L 21/8247, H01L 29/788, H01L 29/792

(21) Application number: **09359258**
(22) Date of filing: **26.12.1997**

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(54) **NON-VOLATILE SEMICONDUCTOR STORAGE**

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a memory cell connecting system in which parasitic capacity of a bit line can be reduced by technology in which connection of memory cells constituting a memory array is hierarchical constitution of a sub-bit line and read-out operation speed can be increased, and a taking method for differential input of a differential type sense amplifier.

SOLUTION: This device is provided with Sid-MOS connecting a main bit line BL and a sub-bit line as a memory cell connecting system and transistor Sid-MOS discharging the sub-bit line. In read-out operation, a gate signal SiDB is a complementary signal of a gate signal Sid of Sid-MOS. Precharge of a read-out bit line and a reference bit line is performed before selecting Sid-MOS using a differential type sense amplifier. Further, this device is provided with a function by which an approximately half current of a memory cell is made to flow to a read-out bit line in the direction of canceling a memory cell current.